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Memory Window and Endurance Improvement of $Hf_{0.5}Zr_{0.5}O_2$-Based FeFETs with ZrO_2 Seed Layers Characterized by Fast Voltage Pulse Measurements

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Abstract

The HfO_2-based ferroelectric field effect transistor (FeFET) with a metal/ferroelectric/insulator/semiconductor (MFIS) gate stack is currently being considered as a possible candidate for high-density and fast write speed non-volatile memory. Although the retention performance of the HfO_2-based FeFET with a MFIS gate stack could satisfy the requirements for practical applications, its memory window (MW) and reliability with respect to endurance should be further improved. This work investigates the advantage of employing ZrO_2 seed layers on the MW, retention, and endurance of the $Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based FeFETs with MFIS gate stacks, by using fast voltage pulse measurements. It is found that the HZO-based FeFET with a ZrO_2 seed layer shows a larger initial and 10-year extrapolated MW, as well as improved endurance performance compared with the HZO-based FeFET without the ZrO_2 seed layer. The results indicate that employing of a direct crystalline high-k/Si gate stack would further improve the MW and reliability of the HfO_2-based FeFETs.

Keywords: HfO_2-based FeFET, Memory window, Retention, Endurance, ZrO_2 seed layer

Background

HfO_2-based ferroelectric thin films are considered as promising gate-stack materials for ferroelectric field effect transistors (FeFETs) because of their complementary metal-oxide-semiconductor (CMOS) compatibility and scalability. Among several kinds of gate stack structures that can be used in FeFETs, a metal/ferroelectric/insulator/semiconductor (MFIS) represents a more practical configuration because it follows the current MOS device architectures and matches well with the modern high-k metal-gate (HKMG) processes. Therefore, great efforts have been made to design and fabricate FeFETs with MFIS gate stack structures for applications in embedded nonvolatile memories, negative capacitance field effect transistors, artificial neurons, synapses, and logic-in-memory devices [1–8].

Up to now, high-density and fast write speed FeFETs with MFIS gate stack structures have been successfully fabricated using HKMG processes [9, 10]. In addition to the high integration density and fast write speed, a large memory window (MW) and a high reliability with respect to retention and endurance are also critical for employing FeFETs for nonvolatile memory applications [11–14]. Owing to a large band offset to silicon, a high coercive field and a moderate dielectric constant of the HfO_2-based ferroelectric thin films, HfO_2-based FeFETs with MFIS gate stack structures exhibit reliable retention properties (10-year extrapolation) [15–17]. However, although the HfO_2-based thin films demonstrate moderate endurance over 1×10^9 switching cycles [14, 18], HfO_2-based FeFETs with MFIS gate stack structures have a rather limited endurance ranging from 1×10^4 to 1×10^7 switching cycles [17, 19–23]. Theoretically, employing of high-k insulator layers is expected to

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reduce the electric field in the MFIS gate stack, which would alleviate the band bending, thereby improving the endurance properties and the MWs of the HfO_2-based FeFETs [12, 14]. Experimentally, Ali et al. verified that increasing the k value of the ultrathin insulator layer (i.e., using SiON instead of SiO_2) can effectively improve the endurance properties as well as the MW of the HfO_2-based FeFETs [13]. In our previous research [24], we reported that the insertion of a crystalline ZrO_2 high-k layer in the MFIS gate stacks could improve the crystalline quality and suppress the formation of monoclinic phase in $Hf_{0.5}Zr_{0.5}O_2$ (HZO) thin films, which leads to a large MW of 2.8 V characterized by DC voltage sweep method.

In this work, we report on the characterization of the MWs, retention, and endurance of the HZO-based FeFETs with and without crystalline ZrO_2 seed layers by using fast positive and negative voltage pulse measurements. Moreover, the advantage of employing crystalline ZrO_2 seed layers on the MW and endurance properties is discussed.

Methods

The n-channel FeFETs with and without ZrO_2 seed layers were fabricated using a gate last process, as described in [24]. The ZrO_2 seed layer and the HZO layer were both grown at a growth temperature of 300 °C by atomic layer deposition (ALD). The schematic of the fabricated FeFETs is shown in Fig. 1a, whose channel width (W) and length (L) were 80 and 7 μm, respectively. Meanwhile, TaN/HZO/TaN and TaN/HZO/ZrO_2/TaN capacitors were also fabricated to evaluate the ferroelectric properties of the HZO thin films. The polarization–voltage (P–V) hysteresis loops of the capacitors were measured using a Radiant Technologies RT66A ferroelectric test system, while the device characteristics of FeFETs were measured by an Agilent B1500A semiconductor device analyzer with a pulse generator unit (B1525A) [20]. Two main test sequences used for MW and endurance measurements are shown in Fig. 1b and c. For MW and retention measurements, program/erase (P/E) pulses were first applied to the gates of FeFETs, and read operations were performed at different time intervals using I_D–V_G sweep (V_D = 0.1 V) to sense V_{TH}. Generally, V_{TH} is determined as a gate voltage corresponding to a drain current of 10^{-7} A·W/L [25], and the MW is defined as the difference of V_{TH} values between programmed and erased states. For endurance measurements, the MW was measured after a certain number of alternating P/E pulses.

Results and Discussion

Figure 2a shows the P–V hysteresis loops of the TaN/HZO/TaN and TaN/HZO/ZrO_2/TaN capacitors. Remarkably, the TaN/HZO/ZrO_2/TaN capacitor possesses even better ferroelectric properties than the TaN/HZO/TaN capacitor, which is consistent with the reported results [26], indicating that the crystalline ZrO_2 seed layer could indeed improve the crystalline quality and suppress the formation of monoclinic phase in HZO thin films [24]. Figure 2b shows the I_D–V_G curves of the HZO-based FeFETs with and without additional crystalline ZrO_2 seed layers after P/E pulses. The red symbol lines represent the I_D–V_G curves after applying a program pulse of 7 V/100 ns, while the blue symbol lines represent the I_D–V_G curves after applying an erase pulse

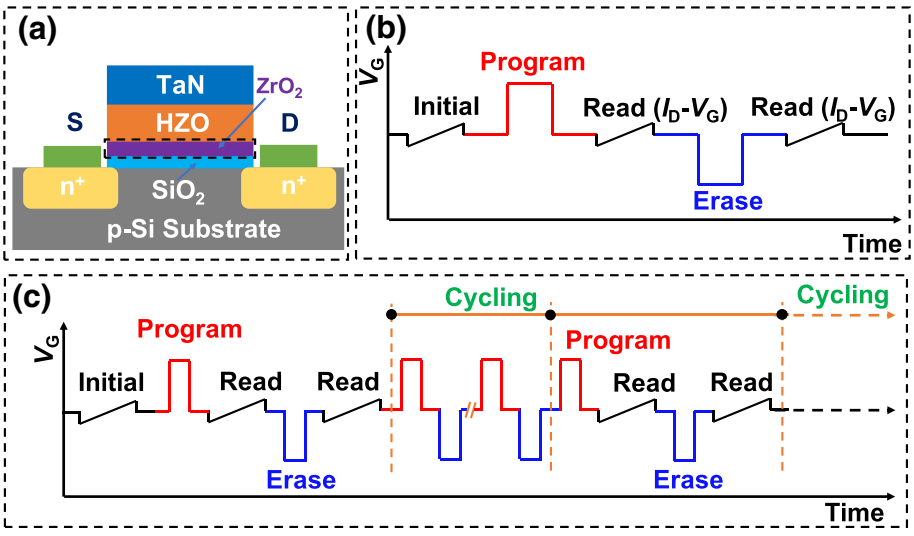

Fig. 1 **a** Schematic of the fabricated FeFETs. The additional crystalline ZrO_2 seed layer is marked by black gridlines. **b**, **c** Test sequences used for MW and endurance measurements

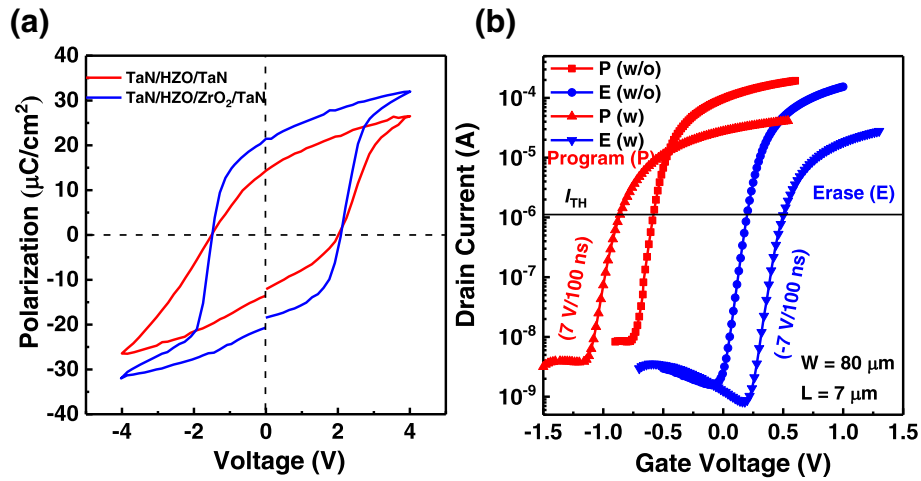

Fig. 2 **a** *P–V* hysteresis loops of TaN/HZO/TaN and TaN/HZO/ZrO_2/TaN MFM structures measured at 4 V and a frequency of 5 kHz. **b** I_D–V_G curves of HZO-based FeFETs with (w) and without (w/o) ZrO_2 seed layers after a program pulse (+ 7 V/100 ns) and an erase pulse (– 7 V/100 ns)

of – 7 V/100 ns. One can see that the I_D–V_G curves of both FeFETs show counterclockwise switching characteristics, suggesting that the MWs of the present FeFETs are originated from the polarization switching of the HZO layers, rather than the charge trapping and injection. Nevertheless, the HZO-based FeFET with the additional crystalline ZrO_2 seed layer exhibits an improved MW of 1.4 V, approximately 1.8 times larger than that (0.8 V) of the HZO-based FeFET without the additional crystalline ZrO_2 seed layer. Moreover, the obtained MW of 1.4 V is comparable to the best results reported to date [9, 11, 14, 17, 21–23, 27].

Reliability with respect to the retention of the HZO-based FeFETs with and without additional crystalline ZrO_2 seed layers was also evaluated. Figure 3 shows the V_{TH} retention characteristics after applying a program pulse of 7 V/100 ns and an erase pulse of – 7 V/100 ns at room temperature. It is clear that the V_{TH} values are approximately linear with the logarithmic time scale. The extrapolated MW after 10 years for the HZO-based FeFET with the additional crystalline ZrO_2 seed layer is 0.9 V, larger than that (0.6 V) for the HZO-based FeFET without the additional crystalline ZrO_2 seed layer. Since the thick capacitance equivalent thickness (CET) of the ZrO_2 (1.5 nm)/SiO_2 (2.6 nm) gate insulator layers would lead to an enhanced depolarization field in the gate stack [13, 15], further improvement in retention properties could be expected if the thickness of the SiO_2 layer is reduced.

Figure 4 shows the evolution of I_D–V_G curves after ± 7 V/100 ns alternating P/E cycles. For the FeFET without the additional crystalline ZrO_2 seed layer, both significant shift and slope degradation in the I_D–V_G curves are observed from the early stages of P/E cycling, and the I_D–V_G curves in the erased states exhibit more slope degradation compared with the program states. For the FeFET with the additional crystalline ZrO_2 seed layer, although the I_D–V_G curves in erased states exhibit an obvious positive shift during the early stages of P/E cycling that is attributed to the "wake up" effect [13, 28–32], no obvious shift of I_D–V_G curves in the program states is observed up to 1×10^3 cycles. Moreover, for the FeFET with the additional crystalline ZrO_2 seed layer, the I_D–V_G curves in both erased and program states exhibit only a slight slope degradation up to 1×10^3 cycles.

According to previous reports [12, 28, 33], the parallel shift in I_D–V_G curves is attributed to the gradual accumulation of trapped charges in the gate stack, while the slope degradation in I_D–V_G curves is the result of interface trap generation. Since trapped charges can be detrapped by electrical means, but generation of interface

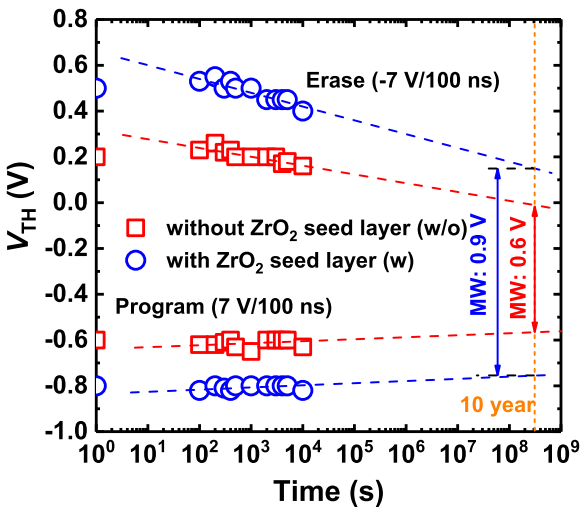

Fig. 3 Retention characteristics of HZO-based FeFETs with and without ZrO_2 seed layers

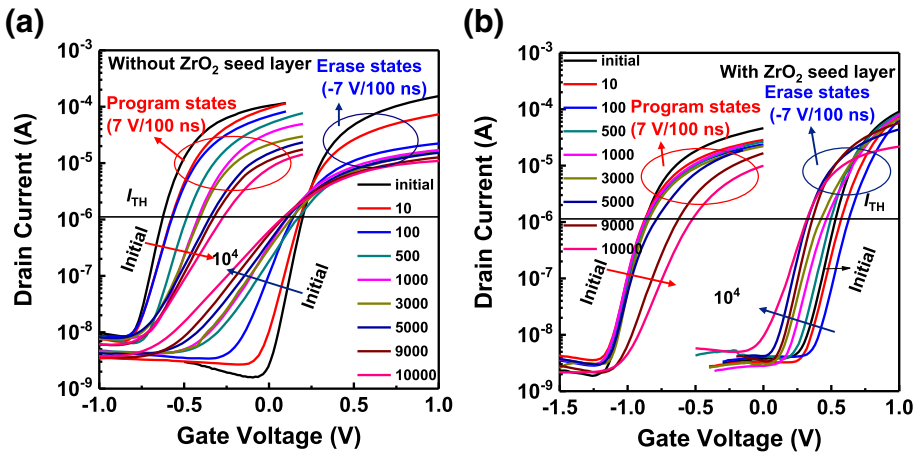

Fig. 4 Evolution of I_D–V_G curves of HZO-based FeFETs **a** without and **b** with ZrO_2 seed layers with P/E cycling

traps is irreversible, minimizing interface trap generation is extremely important for improving the endurance properties [28]. The interface traps generated by P/E cycling (ΔN_{it}) can be described using Eq. (1) [34, 35]:

$$\Delta SS = \frac{\Delta N_{it} kT \ln 10}{C_{FI} \varnothing_F} \quad (1)$$

where ΔSS is the change of the subthreshold swing, k is the Boltzmann constant, T is the absolute temperature, C_{FI} is the total capacitance of gate stack, and $\varnothing_F$ is the Fermi potential. The ΔN_{it} as a function of the P/E cycle for the HZO-based FeFETs with and without additional crystalline ZrO_2 seed layers is shown in Fig. 5. Clearly, for the FeFET without the additional crystalline ZrO_2 seed layer, the ΔN_{it} increases obviously from the early stages of the P/E cycling, and ΔN_{it} in the erased states is much larger than that in the program states. However, the ΔN_{it} for the FeFET with the additional crystalline ZrO_2 seed layer almost does not change up to 1×10^3 cycles, and it is always smaller than that for the FeFET without the additional crystalline ZrO_2 seed layer. Because inserting the additional ZrO_2 seed layer reduces the electric field in the gate stack and thus the band bending is weaker, the interface trap generation is alleviated [12, 14].

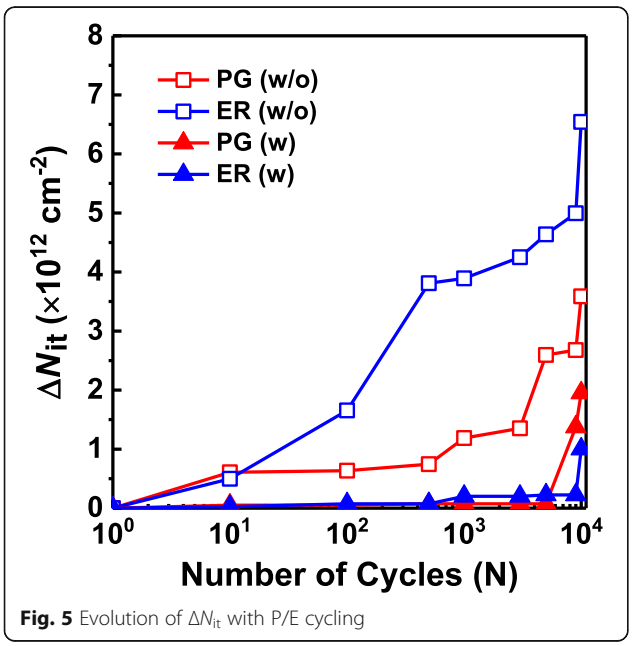

Fig. 5 Evolution of ΔN_{it} with P/E cycling

Figure 6 shows the evolution of gate leakage current characteristics (I_G–V_G curves) of HZO-based FeFETs with and without ZrO_2 seed layers with P/E cycling. For the FeFET without the additional crystalline ZrO_2 seed layer, the gate leakage current increases dramatically from the early stages of the P/E cycling. However, the gate leakage current for the FeFET with the additional crystalline ZrO_2 seed layer almost does not change up to 5×10^2 cycles, and it is always smaller than that for the FeFET without the additional crystalline ZrO_2 seed layer. It is reported that the increase in the gate leakage current might be related to the generated interface traps [28]. The reduction in the gate leakage current with cycling for the FeFET with the additional crystalline ZrO_2 seed layer would be attributed to the suppression of interface trap generation.

The V_{TH} values for program and erase states extracted from the I_D–V_G curves of the HZO-based FeFETs with and without additional crystalline ZrO_2 seed layers are shown in Fig. 7. The HZO-based FeFET with the additional crystalline ZrO_2 seed layer always exhibits a larger MW than the HZO-based FeFET without the additional crystalline ZrO_2 seed layer. Moreover, the MW of the HZO-based FeFET without the additional crystalline ZrO_2 seed layer decreases obviously from the early stages of P/E cycling, while the MW of the HZO-based FeFET with the additional crystalline ZrO_2 seed layer decreases slightly up to 1×10^3 cycles. As the P/E cycling number is further increased, the HZO-based

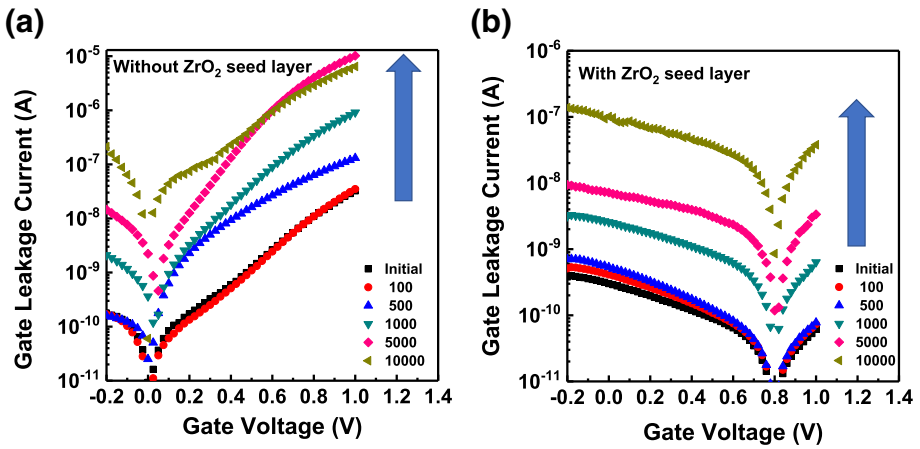

Fig. 6 Evolution of gate leakage current characteristics (I_G–V_G curves) of HZO-based FeFETs **a** without and **b** with ZrO_2 seed layers with P/E cycling

FeFET with the additional crystalline ZrO_2 seed layer also shows obvious degradation in the slope of the I_D–V_G curves and the MW, due to the enhanced generation of interface traps. However, the MW of the HZO-based FeFET with the additional crystalline ZrO_2 seed layer is still larger than 0.9 V up to 1×10^4 cycles, which is approximately 2.3 times larger than that (0.4 V) of the HZO-based FeFET without the additional crystalline ZrO_2 seed layer. As discussed previously, the decrease of the required electric field for obtaining more saturated polarization states are probably responsible for the improved endurance properties.

Conclusions

The MWs as well as the reliability with respect to retention and endurance of the HZO-based FeFETs with the TaN/HZO/SiO_2/Si and TaN/HZO/ZrO_2/SiO_2/Si MFIS gate stacks were characterized by fast voltage pulse measurements. The results show that the HZO-based FeFET with the additional crystalline ZrO_2 seed layer exhibits a large initial memory window of 1.4 V and an extrapolated 10-year retention of 0.9 V, larger than the initial memory window (0.8 V) of the HZO-based FeFET without the additional crystalline ZrO_2 seed layer. Moreover, the reliability with respect to the endurance of the HZO-based FeFET can be improved by inserting the crystalline ZrO_2 seed layer in between the HZO layer and the SiO_2/Si substrate. The MW and endurance improvement of HZO-based FeFETs with ZrO_2 seed layers are primarily related to the improved crystalline quality of the HZO layer and the suppressed generation of interface traps due to the decrease of the required electric field for obtaining more saturated polarization states. On the basis of this work, it is expected that employing of a direct crystalline high-k/Si gate stack would further improve the MWs and reliability of the HfO_2-based FeFETs, and thus warrant further study and development.

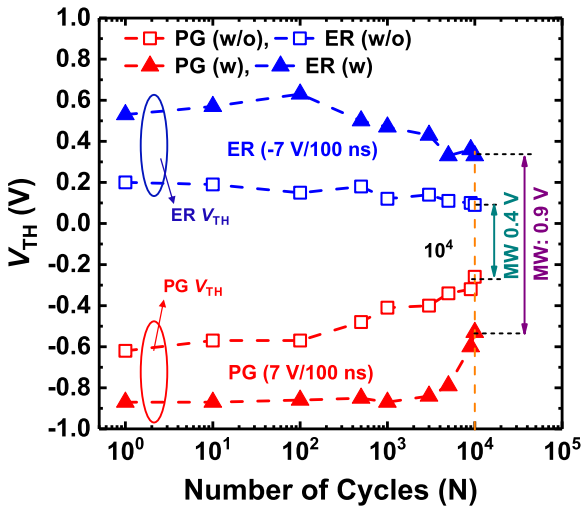

Fig. 7 Evolution of V_{TH} with P/E cycling

Abbreviations

CMOS: Complementary metal-oxide-semiconductor; FeFET: Ferroelectric field effect transistor; FeFETs: Ferroelectric field effect transistors; HKMG: High-k metal-gate; HZO: $Hf_{0.5}Zr_{0.5}O_2$; I_D: Drain current; L: Length; MFIS: Metal/ferroelectric/insulator/semiconductor; MW: Memory window; P/E: Program/erase; *P*–*V*: Polarization–voltage; *SS*: Subthreshold swing; V_G: Gate voltage; V_{TH}: Threshold voltage; W: Width; ΔN_{it}: The generated interface traps

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Not applicable.

Authors' Contributions

WWX carried out the experiments and drafted the manuscript. WWX and CL did the data analysis and interpreted the results. WWX, ML, YP, and SZZ designed the experiments. CL helped to measure the device. ML and SZZ helped to revise the manuscript. WWX, CL, and ML participated in the discussion of results. QF, CFZ, JCZ, YH, and YCZ supported the study. All the authors read and approved the final manuscript.

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Availability of Data and Materials
The datasets supporting the conclusions of this article are included within the article.

Competing Interests
The authors declare that they have no competing interests.

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References

1. Mulaosmanovic H, Chicca E, Bertele M, Mikolajick T, Slesazeck S (2018) Mimicking biological neurons with a nanoscale ferroelectric transistor. Nanoscale 10:21755–21763
2. Mulaosmanovic H, Mikolajick T, Slesazeck S (2018) Accumulative polarization reversal in nanoscale ferroelectric transistors. ACS Appl Mater Interfaces 10: 23997–24002
3. Mulaosmanovic H, Ocker J, Müller S, Noack M, Müller J, Polakowski P, Mikolajick T, Slesazeck S (2017) Novel ferroelectric FET based synapse for neuromorphic systems. In: Symposium on VLSI Technology, pp 176–177
4. Hoffmann M, Pešic M, Chatterjee K, Khan AI, Salahuddin S, Slesazeck S, Schröder U, Mikolajick T (2016) Direct observation of negative capacitance in polycrystalline ferroelectric HfO_2. Adv Funct Mater 26:8643–8649
5. Lee MH, Wei YT, Chu KY, Huang JJ, Chen CW, Cheng CC, Chen MJ, Lee HY, Chen YS, Lee LH, Tsai MJ (2015) Steep slope and near non-hysteresis of FETs with antiferroelectric-like HfZrO for low-power electronics. IEEE Electron Device Lett. 36:294–296
6. Yin X, Aziz A, Nahas J, Datta S, Gupta S, Niemier M, Hu XS (2016) Exploiting ferroelectric FETs for low-power non-volatile logic-in-memory circuits. In: Proc IEEE/ACM Int. Conf. Comput.-AidedDesign (ICCAD), pp 1–8
7. Breyer ET, Mulaosmanovic H, Mikolajick T, Slesazeck S (2018) Reconfigurable NAND/NOR logic gates in 28 nm HKMG and 22 nm FD-SOI FeFET technology. In: IEEE International Electron Devices Meeting (IEDM), pp 28.5.1–28.5.4
8. Zhou JR, Han GQ, Xu N, Li J, Peng Y, Liu Y, Zhang JC, Sun Q-Q, Zhang DW, Hao Y (2019) Incomplete dipoles flipping produced near hysteresis-free negative capacitance transistors. IEEE Electron Device Lett. 40:329–332
9. Müller J, Yurchuk E, Schlösser T, Paul J, Hoffmann R, Müller S, Martin D, Slesazeck S, Polakowski P, Sundqvist J, Czernohorsky M, Seidel K, Kücher P, Boschke R, Trentzsch M, Gebauer K, Schröder U, Mikolajick T (2012) Ferroelectricity in HfO_2 enables nonvolatile data storage in 28 nm HKMG. In: Symposium on VLSI Technology (VLSIT), pp 25–26
10. Trentzsch M, Flachowsky S, Richter R, Paul J, Reimer B, Utess D, Jansen S, Mulaosmanovic H, Müller S, Slesazeck S, Ocker J, Noack M, Müller J, Polakowski P, Schreiter J, Beyer S, Mikolajick T, Rice B (2016) A 28 nm HKMG super low power embedded NVM technology based on ferroelectric FETs. In: IEEE International Electron Devices Meeting (IEDM), pp 11.5.1–11.5.4
11. Dünkel S, Trentzsch M, Richter R, Moll P, Fuchs C, Gehring O, Majer M, Wittek S, Müller B, Melde T, Mulaosmanovic H, Slesazeck S, Müller S, Ocker J, Noack M, Löhr D-A, Polakowski P, Müller J, Mikolajick T, Höntschel J, Rice B, Pellerin J, Beyer S (2017) A FeFET based super-low-power ultra-fast embedded NVM technology for 22 nm FDSOI and beyond. In: IEEE International Electron Devices Meeting (IEDM), pp 19.7.1–19.7.4
12. Müller J, Polakowski P, Müller S, Mulaosmanovic H, Ocker J, Mikolajick T, Slesazeck S, Müller S, Ocker J, Mikolajick T, Flachowsky S, Trentzsch M (2016) High endurance strategies for hafnium oxide based ferroelectric field effect transistor. In: Proc. IEEE Non-Volatile Memory Technol. Symp. (NVMTS), pp 1–7
13. Ali T, Polakowski P, Riedel S, Büttner T, Kämpfe T, Rudolph M, Pätzold B, Seidel K, Löhr D, Hoffmann R, Czernohorsky M, Kühnel K, Steinke P, Calvo J, Zimmermann K, Müller J (2018) High endurance ferroelectric hafnium oxide-based FeFET memory without retention penalty. IEEE Trans Electron Devices 65:3769–3774
14. Ni K, Sharma P, Zhang JC, Jerry M, Smith JA, Tapily K, Clark R, Mahapatra S, Datta S (2018) Critical role of interlayer in $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric FET nonvolatile memory performance. IEEE Trans Electron Devices 65:2461–2469
15. Gong N, Ma T-P (2016) Why Is FE–HfO_2 more suitable than PZT or SBT for scaled nonvolatile 1-T memory cell? A retention perspective. IEEE Electron Device Lett 37:1123–1126
16. Müller J, Polakowski P, Mueller S, Mikolajick T (2015) Ferroelectric hafnium oxide based materials and devices: assessment of current status and future prospects. ECS J Solid State Sci Technol 4:30–35
17. Müller J, Boscke TS, Schröder U, Hoffmann R, Mikolajick T, Frey L (2012) Nanosecond polarization switching and long retention in a novel MFIS-FET based on ferroelectric HfO_2. IEEE Electron Device Lett 33:185–187
18. Müller S, Müller J, Schröder U, Mikolajick T (2013) Reliability characteristics of ferroelectric Si: HfO_2 thin films for memory applications. IEEE Trans. Device Mater Reliab 13:93–97
19. Müller S, Summerfelt SR, Müller J, Schröder U, Mikolajick T (2012) Ten-nanometer ferroelectric Si: HfO_2 films for next-generation FRAM capacitors. IEEE Electron Device Lett. 33:1300–1302
20. Zeng BJ, Xiao WW, Liao JJ, Liu H, Liao M, Peng QX, Zheng SZ, Zhou YC (2018) Compatibility of HfN metal gate electrodes with $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric thin films for ferroelectric field-effect transistors. IEEE Electron Device Lett 39:1508–1511
21. Yurchuk E, Müller J, Paul J, Schlösser T, Martin D, Hoffmann R, Müeller S, Slesazeck S, Schröeder U, Boschke R, Bentum RV, Mikolajick T (2014) Impact of scaling on the performance of HfO_2-based ferroelectric field effect transistors. IEEE Trans. Electron Devices 61:3699–3706
22. Chen KT, Chen HY, Liao CY, Siang GY, Lo C, Liao MH, Li KS, Chang ST, Lee MH (2019) Non-volatile ferroelectric FETs using 5-nm $Hf_{0.5}Zr_{0.5}O_2$ with high data retention and read endurance for 1 T memory applications. IEEE Electron Device Lett. 40:399–402
23. Chatterjee K, Kim S, Karbasian G, Tan AJ, Yadav AK, Khan AI, Hu CM, Salahuddin S (2017) Self-aligned, gate last, FDSOI, ferroelectric gate memory device with 5.5-nm $Hf_{0.8}Zr_{0.2}O_2$, high endurance and breakdown recovery. IEEE Electron Device Lett 38:1379–1382
24. Xiao WW, Liu C, Peng Y, Zheng SZ, Feng Q, Zhang CF, Zhang JC, Hao Y, Liao M, Zhou YC (2019) Performance improvement of $Hf_{0.5}Zr_{0.5}O_2$ based ferroelectric-field-effect transistors with ZrO_2 seed layers. IEEE Electron Device Lett. 40:714–717
25. Ortiz-Conde A, Sánchez FJG, Liou JJ, Cerdeira A, Estrada M, Yue Y (2002) A review of recent MOSFET threshold voltage extraction methods. Microelectron Reliab 42:583–596
26. Onaya T, Nabatame T, Sawamoto N, Ohi A, Ikeda N, Chikyow T, Ogura A (2017) Improvement in ferroelectricity of $Hf_xZr_{1-x}O_2$ thin films using ZrO_2 seed layer. Appl Phys Express 10:081501–1–081501–4
27. Cheng CH, Chin A (2014) Low-leakage-current DRAM-like memory using a one-transistor ferroelectric MOSFET with a Hf-based gate dielectric. IEEE Electron Device Lett. 35:138–140
28. Yurchuk E, Mueller S, Martin D, Slesazeck S, Schröeder U, Mikolajick T, Müller J, Paul J, Hoffmann R, Sundqvist J, Schlösser T, Boschke R, Bentum RV, Trentzsch M (2014) Origin of the endurance degradation in the novel HfO_2-based 1 T ferroelectric non-volatile memories. In: IEEE International Reliability Physics Symposium (IRPS), pp 2E.5.1–2E.5.5
29. Pešic M, Fengler F, Larcher L, Padovani A, Schenk T, Grimley ED, Sang XH, LeBeau JM, Slesazeck S, Schroeder U, Mikolajick T (2016) Physical mechanisms behind the field-cycling behavior of HfO_2-based ferroelectric capacitors. Adv Funct Mater 26:4601–4612
30. Zhou DY, Xu J, Li Q, Guan Y, Cao F, Dong XL, Müller J, Schenk T, Schröder U (2013) Wake-up effects in Si-doped hafnium oxide ferroelectric thin films. Appl Phys Lett 103:192904
31. Kim HJ, Park MH, Kim YJ, Lee YH, Moon T, Kim KD, Hyun SD, Hwang CS (2018) A study on the wake-up effect of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ films by pulse-switching measurement. Nanoscale 8:1383–1389
32. Park MH, Kim HJ, Kim YJ, Lee YH, Moon T, Kim KD, Hyun SD, Hwang CS (2015) Study on the size effect in $Hf_{0.5}Zr_{0.5}O_2$ films thinner than 8 nm before and after wake-up field cycling. Appl Phys Lett 107:192907

33. Gong N, Ma T-P (2018) A study of endurance issues in HfO_2-based ferroelectric field effect transistors: charge trapping and trap generation. IEEE Electron Device Lett 39:15–18
34. Enlow EW, Pease RL, Alexander DR (1987) Subthreshold technique for fixed and interface trapped charge separation in irradiated MOSFETs, Mission Research Corp. Tech. Rep, Albuquerque
35. Zhu WJ (2003) Hafnium oxide and hafnium aluminum oxide for CMOS application. Ph.D. dissertation (Chapter 2). Dept. Elect. Eng., Yale Univ, New Haven

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